IMPLEMENTATION OF MODERN DRAM USING CMOS TECHNOLOGY

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Abstract—Large DRAM arrays that are widely used as main memory in processors and application-specific integrated circuits can occupy a significant portion of the die area. In an attempt to optimize the performance of such chips, large arrays of fast DRAM help to boost the system performance. The area impact of incorporating large DRAM arrays into a chip directly translates into a higher chip cost. Balancing these requirements is driving the effort to minimize the footprint of DRAM cells. As a result, millions of minimum-size DRAM cells are tightly packed making DRAM array the densest circuitry on a chip. The demand for dynamic random-access memory (DRAM) is increasing with large use of DRAM in mobile products, System On-Chip (SoC) and high-performance VLSI circuits.70% of the System on- Chip (SoC) uses DRAM memory. DRAM is significant component used for the main memory in microprocessors, main frame computers, engineering workstations and memory in hand-held devices due to high speed and low power consumption.
The main objective of this paper is to design and implement DRAM Memory array using 180nm CMOS technology. The work includes designing of write driver circuit, pre-charge circuit, memory cell, Sense amplifier and row decoder. The DRAM Memory array (4x4) is capable of storing 16 bits(2 bytes) with operating voltage of 1.8v.To design and implement DRAM Memory array Standard gpdk180 (General Purpose Design Kit) technology library is used .The proposed work is designed using Cadence Tool.

Key Words—DRAM, array, cadence, voltage, power

I. INTRODUCTION

In dynamic RAM, a single memory cell is therefore, implemented using a single transistor and a capacitor which occupy lesser space as compared to six transistor which are used to implement a single static cell. Therefore, the density of capacitor based memory is significantly increased. The capacitor based memory is known as dynamic RAM (DRAM). The advantage of a DRAM is the simplicity of the cell - it only requires a single transistor compared to around six in a typical static RAM, DRAM memory cell. N view of its simplicity, the costs of DRAM are much lower than those for DRAM, and they are able to provide much higher levels of memory density. And as a result, most computers use both DRAM technology and DRAM, but in different areas. In view of the fact that power is required for the DRAM to maintain its data, it is what is termed a volatile memory.

II. BASIC DRAM CELL

DRAM (Dynamic Random Access Memory) is the main memory used for all desktop and larger computers. Each elementary DRAM cell is made up of a single MOS transistor and a storage capacitor (Figure 1). Each storage cell contains one bit of information. This charge, however, leaks off the capacitor due to the sub-threshold current of the cell transistor. Therefore, the charge must be refreshed several times each second. The memory cell is written to by placing a “1” or “0” charge into the capacitor cell. This is done during a write cycle by opening the cell transistor (gate to power supply or VCC) and presenting either VCC or 0V (ground) at the capacitor. The word line (gate of the transistor) is then held at ground to isolate the capacitor charge. This capacitor will be accessed either for a new write, a read or a refresh.

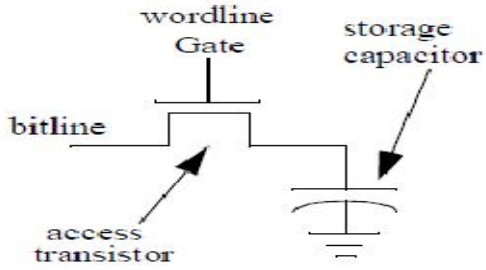


Figure1.DRAM cell

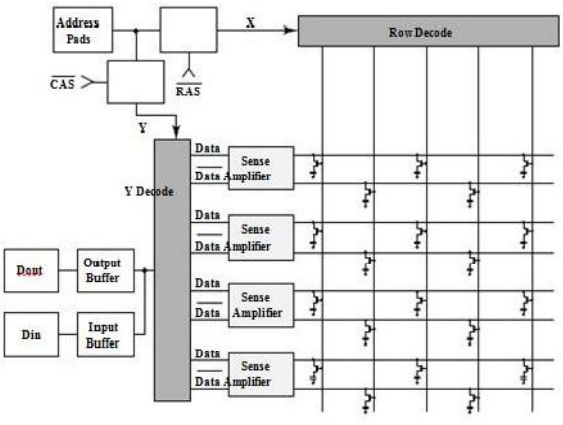


Figure2. Simplified DRAM block diagram

Row addresses are present on address pads and are internally validated by the RAS (Row Address Access) clock. A bar on top of the signal name means this signal is active when it is at a low level. The X addresses select one row through the row decode, while all the other non-selected rows remain at 0V. Each cell of the selected row is tied to a sense amplifier. A sense amplifier is a circuit that is able to recognize if a charge has been loaded into the capacitor of the memory cell, and to translate this charge or lack of charge into a 1 or 0. Each sense amplifier is connected to a column . In this first step all the cells of the entire row are read by the sense amplifier. This step is long and critical because the row has a high time constant due to the fact that it is formed by the gates of the memory cells. Also, the sense amplifier has to read a very weak charge (approximately 30 fem to Farads or 50fF).

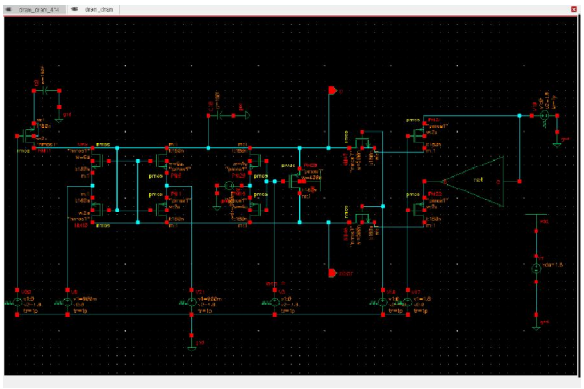


Figure3. 1 bit schematic for DRAM

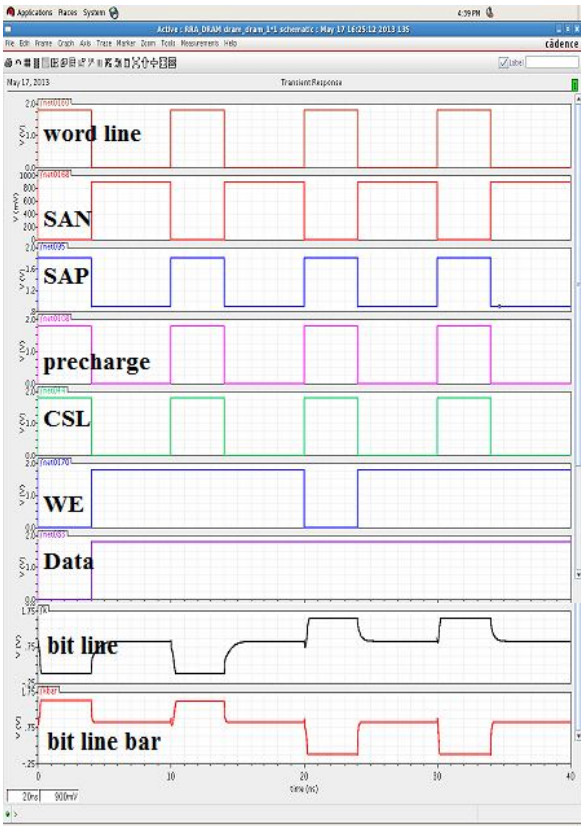


Figure 4.Output waveforms for 1 bit schematic

The figure 3 shows the schematic for the 1 bit dram with its control circuitry. Consist of sense amplifier, pre-charge column selector and write enable circuit. Concerned figure4 is an input and output waveforms with all control signals. This works on the 5 phases. That is precharge, access, sense, restore, and write.

The precharge phase is typically considered as a separate operation from a row access operation. That is, while the Precharge phase is a prerequisite for the subsequent phases of a row access operation, it is typically performed separately from the row access. On the other hand, Access, Sense, and Restore are three different phases that are performed atomically in sequence for any row access operation. Phase zero illustrates that before the process of reading data from a DRAM array can begin, the bit lines in a DRAM array is precharged to a reference voltage, Vref. In many modern DRAM devices, Vcc/2, the voltage half way between the power supply voltage and ground, is used as the reference voltage. the equalization circuit is activated, and the bit lines are precharged to Vref.

Phase one is a (cell) Access, and it illustrates that as a voltage is applied to the right most word line, that word line is overdriven to a voltage that is at least Vt above Vcc. The voltage on the word line activates the access transistors, and the charge in the storage cell is discharged onto the bitline. In this case, since the voltage in the storage cell was a high voltage value that represented a digital value of “1”, the voltage on the bitline increases from Vref to Vref +. As the voltage on the bitline changes, the higher voltage on the bitline begins to affect operations of the cross connected sensing circuit. In the case the slightly higher voltage on the bitline begins to drive the lower NFet to be more conductive than the upper NFet. Conversely, the minute voltage difference drives the lower PFet to be less conductive than the upper PFet. The bit line voltage thus biases the sensing circuit and readies it for the sensing phase. the minute voltage differences drives a bias into the cross connected sensing circuit, SAN, the DRAM device’s Nsense amplifier control signal, turns on and drives the voltage on the lower bitline down. SAN turns on, the more conductive lower NFet allows SAN to drive the lower bitline down in voltage from Vref to ground. Similarly, SAP, the Psense amplifier control signal drives the bitline to a fully restored voltage value that represents the digital value of “1”. The SAN and SAP control signals thus collectively force the bi-stable sense amplifier circuit to be driven to the respective maximum or minimum voltages.

In the restore phase after the bitlines are driven to the respective maximum or minimum voltage values, the overdriven word line remains active and the fully driven bitline voltage now restores the charge in the storage capacitor through the access transistor. At the same time, the voltage value on the bit line can be driven out of the sense amplifier circuit to provide the requested data. In this manner, the contents of a DRAM row can be accessed and driven out of the

DRAM device concurrently with the data restoration process.

In the write phase data is automatically restored from the sense amplifiers to DRAM cells. However, in the case of a write command in commodity DRAM devices, data written by the memory controller is buffered by the I/O buffer of the DRAM device and used to overwrite the sense amplifiers and DRAM cells. In this case, the restore phase may be extended by the write recovery phase. Similar to the relative timing described in Figure 4, the addition of a column write command simply means that a precharge command cannot be issued until after the correct data values have been restored to the DRAM cells. The time period required for write data to overdrive the sense amplifiers and through written to the DRAM cells is referred to as the write recovery time.

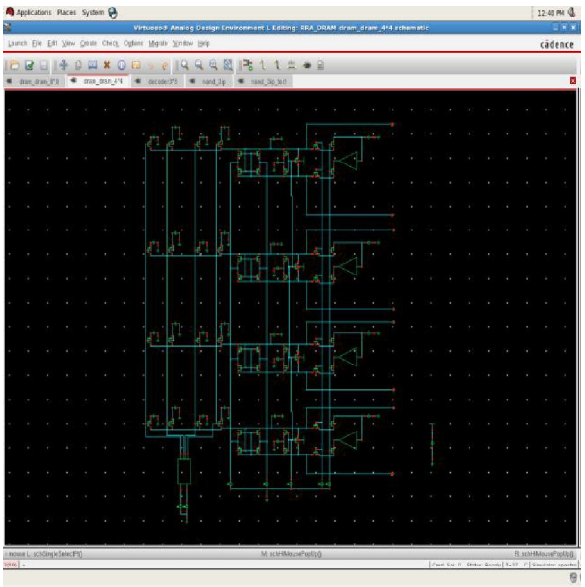
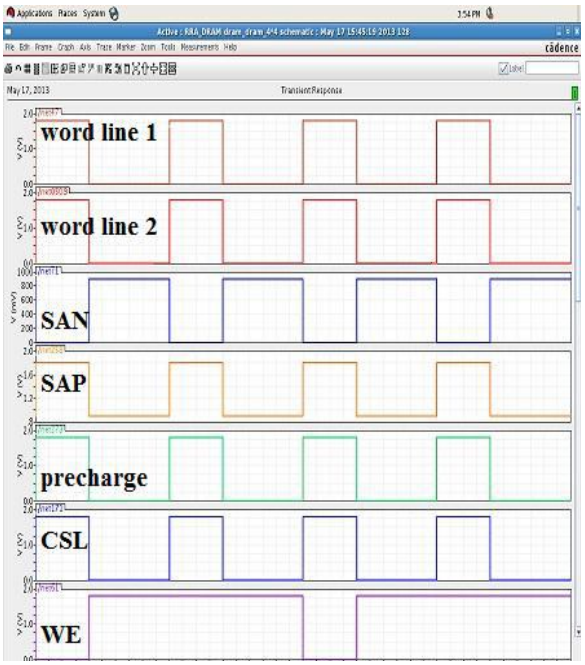


Figure 5.schematic for 4x4 modern DRAM



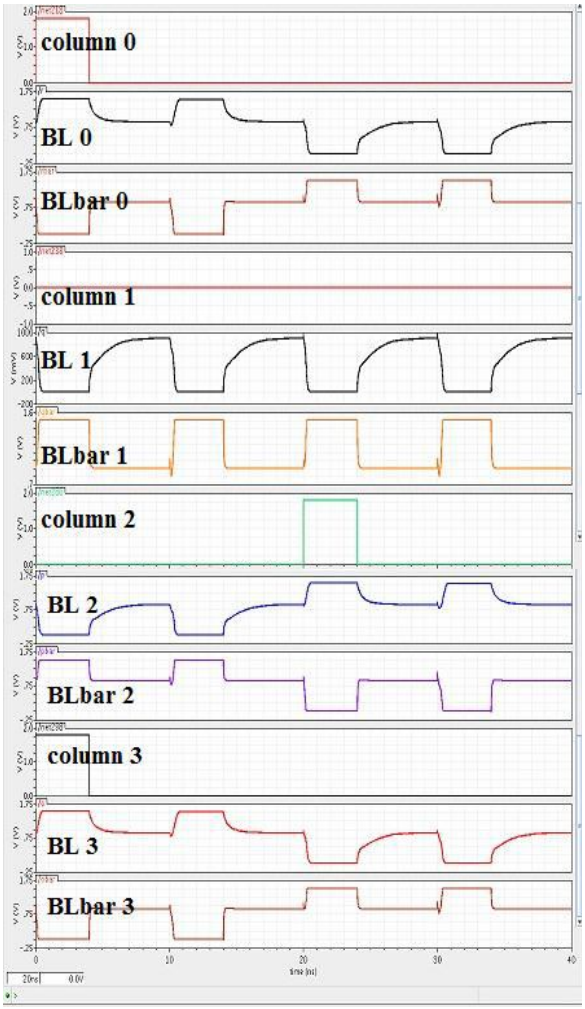


Figure 6.output for 4x4 modern DRAM

The Figure 4 shows the schematic for the 4x4 DRAM. The each column consists of 4 DRAM cells having a single control circuitry. Hence for DRAM array 4*4 four control circuit is required for each column. The corresponding output for 4*4 array is shown in the figure 5. In the figure 5 the input and output relations is given for each column.

III. UNITS

1nm=10-9m.
1pF=10-12F.
1fF=10-15F.

IV. HELPFUL HINTS

Figure1: DRAM cell.
Figure2: Simplified DRAM block diagram.
Figure3: 1 bit schematic for DRAM.
Figure4: Output waveforms for 1 bit schematic.
Figure5: Schematic for 4x4 modern DRAM.
Figure6: Output waveform for 4x4 modern DRAM.

V. ABBREVIATIONS

DRAM-Dynamic Random Access Memory

SAN-Sense Amplifier Negative
SAP-Sense Amplifier Positive
CSL-Column Select Line
WE-Write Enable
EQ-Equalization

CONCLUSION

This paper discusses the overall contribution of the project. The schematic is designed for storage capacity of 16 bits i.e., 4x4 Memory array. The design for various arrays is functionally verified and it is observed that the values of column capacitors, and number of control circuits increases as the storage capacity increases. The schematic for 1 bit and 4x4 Memory array which includes peripheral components such as memory bit cell, write driver circuit, pre-charge circuit, sense amplifier are designed and integrated. The integrated DRAM Memory is capable of storing 16bits and automatic refreshable. The proposed work is operated with supply voltage 1.8v.The DRAM is designed and implemented in standard gpdk180nm technology using Cadence virtuoso editor for schematic.

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