DESIGNING OF CURRENT MODE INSTRUMENTATION AMPLIFIER FOR BIO-SIGNAL USING 180NM CMOS TECHNOLOGY

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Abstract—In this paper we have describes the design of current mode instrumentation amplifier (CMIA) for bio-signal Acquisition system. The current mode instrumentation amplifier technology is based on voltage mode operational amplifier (op amp) power supply current sensing technique. There are two design challenges of this topology. First one is the Op amp mismatch and second is precise current mirrors. A new low-voltage single-power high CMRR and PSRR instrumentation amplifier is developed for medical applications. This proposed circuit uses a new structure to solve the general circuit's problems. The overall proposed circuits by virtuoso 6.1.5 using UMC 0.18um CMOS technology achieve a very high CMRR 130dB up to 87 HZ and higher than 100dB up to 10k Hz and PSRR 110 dB up to 1k Hz and 39 dB closed loop gain at 1.8V single power supply

Keywords— Sample and hold (S/H), ADC, PSRR, CMRR, gain bandwidth product (GBW), trans conductance

I. INTRODUCTION

The biomedical signals have a very weak amplitude medical specialty of few Millis -volts or less and also the frequency below 1 kHz [4]. Fig. 1 shows the diagram of complete system used for biomedical detection. Electrodes, amplifier, LPF, Sample and hold (S/H) and ADC are the mail blocks of this method. Since medical specialty electronics is just too weak to observe the medicine signals it's it is that the common mode nose should be minimize and amplify the medicine signal solely, therefore we'd like a correct, high CMRR, and high gain amplifier. The output of the instrumentation gone through more experienced filter, programmable gain amplifier, sample and hold circuit and analog to digital convertor, then these digital information are processed in PC to extract the tiny low frequency differential Signals out from massive common mode interference of human body. Current mode instrumentation amplifier (CMIA) has no complicated resistor network, high gain bandwidth product (GBW), freelance voltage gain and high CMRR that is freelance of differential gain thus it is a lot of advantageous than the standard Instrumentation amplifier. The CMIA topology involves operational electronic equipment (op-amp) power supply current sensing technique. This method is 1st first by B. Wilson, then developed as a current mode amplifier and an instrumentation amplifier . Later and recently, this Current mode instrumentation amplifier topology is further developed and reported by several works [1]-[3]. A comprehensive and elaborate analysis of this CMIA is given in [4]. This paper describes the design of Current mode instrumentation amplifier in a CMOS 180nm technology.

II. INSTRUMENTATION AMPLIFIER

Many industrial and medical applications use instrumentation amplifiers (INAs) to condition small signals within the presence of huge common-mode voltages and DC potentials .The instrumentation amplifier is employed wherever there is a requirement for the amplification of small differential sensing element voltages.

However, the differential sensing element signal is usually in the course of interference within the variety of common-mode voltages at the inputs [2].An amplifier with high CMRR is appropriate for such applications. Such amplifier with programmable gain associated high input impedance is an instrumentation amplifier [1, 2, 3].Most of the instrumentation amplifier uses three-op-amp differential amplifier with resistive feedback, however there is a significant disadvantage of such configuration , that high CMRR performance is related to resistors matching. Some resistors should be cut accurately minimize the common-mode gain, therefore increasing the value of the IA.

III. THE PROPOSED NSTRUMENTATION AMPLIFIER

The schematic of the projected CMIA topologies has been shown in Fig. 2. This projected IA consists of 3 OP-AMPs, current mirrors and solely few resistors. The numbers of resistors are reduced to resolve the issues in resistors network matching of a traditional IA .This CMIA consists of two input op amps A1 and A2 and a resistor R1 because the differential input stage. A1 and A2 are connected as unit gain buffers to convey the input voltages on resistor R1. Since common mode voltages at the two. terminals of R1 is anticipated to be up to one another, solely differential current I1=Vin+ −Vin_R1 flows through. Current mirrors CM1 and CM2 can copy a Current (I2) as correct as (I1) through R2.therefore, we will get I1 =

I2 = -I3. The output voltage is to unfolded in eq.1 with the schematic of the planned IA shown in Fig. 3

$$V_{out} = -2[(V_{in+} - (V_{in-}) \quad (1)$$

The overall CMRR of instrumentation amplifier is give by a following equation.2

$$CMRR = \frac{A_D}{A_{CM}} = \frac{A_{OL_2} * A_1}{A_{OL_2} - A} \quad (2)$$

A finite CMRR can be achieve if the open loop-gains of the input op-amps are totally different,. The magnitude are often approximated by Equation (2).To achieve a high CMRR, either terribly high open-loop gains should be achieved, or the open-loop gains should be tightly matched. Since very high open-loop gains are tough to attain in low-voltage CMOS processes, If the open-loop gains of input op-amp should be tightly matched. so as to get two identical op-amps, a good deal of your time and energy was spent in the layout design of style. The input referred noise should be terribly tiny for efficient acquisition of the signal that historically asks for larger power consumption [7, 8]. Usually the animal tissue electrocardiogram magnitude varies from 20 μV to five mV. Noise of such amplifiers should be sufficiently less than smallest signal, but these systems area unit very restricted by the background signal. Power savings may be achieved if input referred noise of the electronic equipment may be supported the background signal. The schematic of the OP-AMP is shown in Fig. 4. PMOS with giant gate space is employed because the differential input to reduce to scale back flicker noise contribution by them. The low noise design needs careful sizing and biasing of the input transistors and therefore the load. The noise contribution of various transistors [9] may be reduced by concerning Eqn. 3, Eqn. 4 and table 1.

$$Thermal\ Noise\ PSD = i_{nth}^2 = 4 * k_B * T * \gamma * \quad (3)$$

$$Flicker\ Noise = i_{n\frac{1}{f}}^2 = \frac{K}{C_{ox} * W * L} * g \quad (4)$$

Flicker noise is caused primarily as a result of the interface entices density in NMOS and mobility fluctuations in PMOS. It's a serious concern once planning low frequency circuitry .PMOS is that the most well-liked alternative for the input transistors as flicker noise is found a minimum of one order lower than that of NMOS [7]. Flicker noise may be reduced by increasing the active area of the transistors and by decreasing ,

, ratio for load transistor. The input transconductance should be maximized (large W/L) to attain this, for a given current. Flicker noise may be reduced using circuit techniques as correlative double sampling, chopper stabilization switched biasing etc. however they complicate the design and cause extra power consumption. Flicker noise contribution of input transistor combine will solely be reduced by increasing the gate area (Table. I).

TABLE I. INPUT REFFERED NOISE OPTIMIZATION

Input Reffered noise	Input	Load
Thermal Noise	$\alpha \frac{1}{g_{m\_in}}$	$\alpha \frac{g_{m\_load}}{g_{m\_in}^2}$
Flicker Noise	$\alpha \frac{1}{W_{in} * L_{in}}$	$\alpha \frac{g_{load}^2}{g_{m\_in}^2} * \frac{1}{W_{load} * L_{load}}$

Hence (Win * Lin) product and (Win /Lin) ratio of input pair must be increased. The noise from different transistors is reduced mainly by decreasing their transconductance with reference to the input transconductance. Traditionally it's done by decreasing their W/L ratio and giving additional overdrive voltage for a given bias current. However a limit is superimposed on this technique by the output swing, particularly for submicron CMOS technologies. In our noise reduction technique, we've got additional reduced the transconductance of load transistors by reducing bias current through them. The voltage-in and current-out of the projected OP-AMP construction is shown in Fig.4[6] that consists of 4 stages, the primary stage is a bias circuit and therefore the differential PMOS is employed for the input of the second stage. The differential stage is intended by a folded cascade configuration to extend the open loop gain and to regulate the input common mode voltage of OPAMP simply [6]. The third stage provides a high gain stage. Finally, the last stage of the output stage has VO1 and VO2 as outputs .The specifications of the proposed OP-AMP is shown in table2

TABLE II. SIMULATION RESULTS OF THE INPUT CMOS OP-AMP

Technology	0.18μ
Supply Voltage	1.8v
Bandwidth	184Hz
Power Consumption	50μW
Open Loop Gain(dB)	75.39dB
Phase Margin	66º
CMRR	99.3dB
PSRR	100dB
Input referred noise	5.6μv/sqrt (Hz)
Unity gain bandwidth	1.004MHz
Gain Margin	17 dB

IV. SIMULATION RESULTS OF INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is intended with the CMOS 0.18 µm technology. Fig. 5 contains the open-loop gain of op-amp1 (op-amp2) that is 75dB.The simulations are performed with Specter in analog setting. Fig.8 is the frequency response of instrumentation amplifier that is close to loop gain db and therefore the unity gain bandwidth is around 15.5MHz.The CMIA keeps a CMRR (Fig.9) 130dB up to 87 Hz and better than 100dB up to 10k Hz that satisfies the fundamental standard of medical instruments. Fig 10 shows CMIA holds PSRR beyond 100dB up to 10k Hz. Fig. 11 shows the noise performance. For those applications regarding the signal band lower than 0.1 Hz, the chopping technique is needed to more reduce the noise among this band. The results of the transient IA simulation are shown in Fig.12 the input may be a pulse wave signal with 100Hz frequency and 1mV amplitude. Table 3 provides an outline of the simulation Results.

TABLE III. SIMULATION RESULTS OF THE CMOS INSTRUMENTATION AMPLIFIER

Parameter	Result Acheived
Technology	0.18µm
Supply voltage	1.8 V
Band Width	453KHz
Power Consumption	355µW
Closed Loop gain(dB)	30.06dB
Phase Margin	51"
Gain Margin	16"
Unity Gain Bandwidth	15.21MHz
CMRR(from 1m Hz to 87 Hz)	130 dB
CMRR	(from 87 Hz to 10 KHz)>100dB
PSRR	110 dB
Input Referred Noise@1Hz	2.314uV/sqrt(Hz)
Input Referred Noise@10Hz	57uV/sqrt(Hz)
Slew Rate	+0.8V/µs, -0.8v/µs
Settling Time	500 ns

CONCLUSION

A current mode instrumentation amplifier using op amp power supply current sensing technique for bio-signal acquisition system is enforced and analyzed in a CMOS 0.18µm technology. The proposed circuits mix current mirrors that may manage the matter of resistors matching as within the typical instrumentation amplifier. The Simulation results show that the CMIA demonstrates continuous GBW-independent gain adjustment function and good signal distortion performance. The circuit has 130 dB CMRR up to 87 Hz and keeps a value more than 100 dB up to 10k Hz and Input noise voltage is 57nv/ at 10k Chopping technique is needed to more reduce input noise voltage less than 0.1 Hz. The CMIA consumes solely 355 µ W below a 1.8 V dc supply voltage that is suitable for bio-signal application .The circuit doesn't need advanced op amp design however the matching between op amps plays a crucial role in layout part. The accurate current mirror is the main challenge in schematic part for higher CMRR and higher signal quality.

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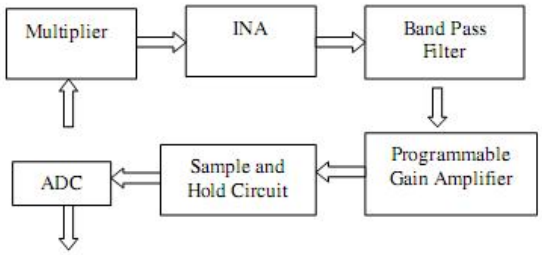

Figure1. The Biomedical Electronics Detecting System Blocks

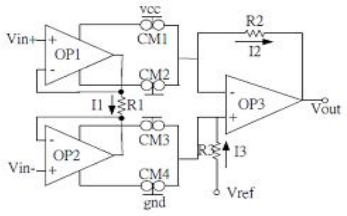

Figure 2.Current mode instrumentation amplifier topology

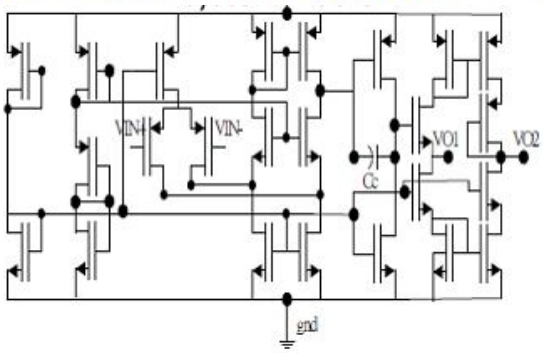

Figure3. Schematic of the proposed Instrumentation amplifier

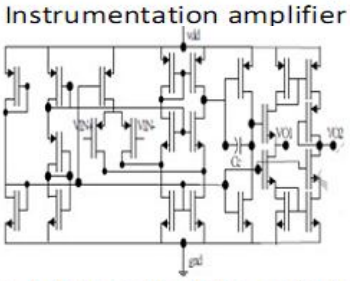

Figure 4. Schematic of the projected input Amp of Instrumentation amplifier

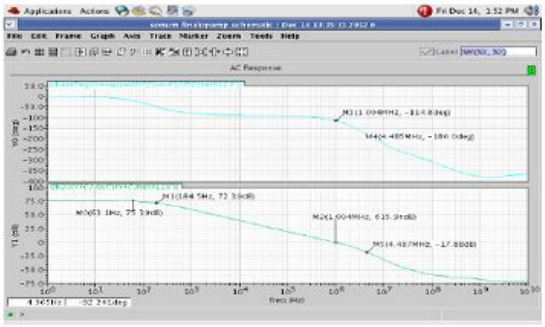

Figure 5. Frequency Response of input op-amp

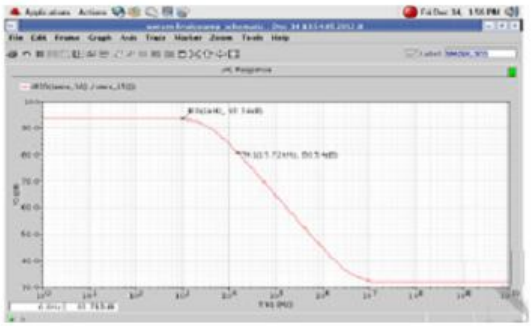

Figure 6. CMRR Frequency Response of input op-amp

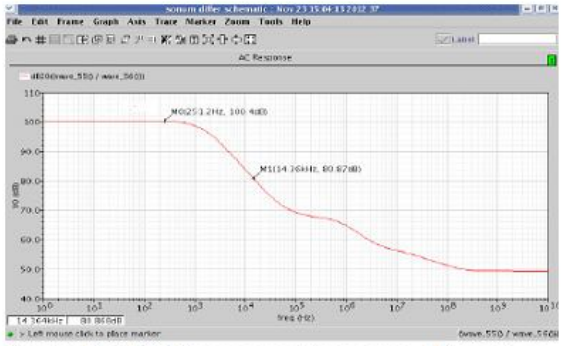

Figure 7. PSRR Frequency Response of input op-amp

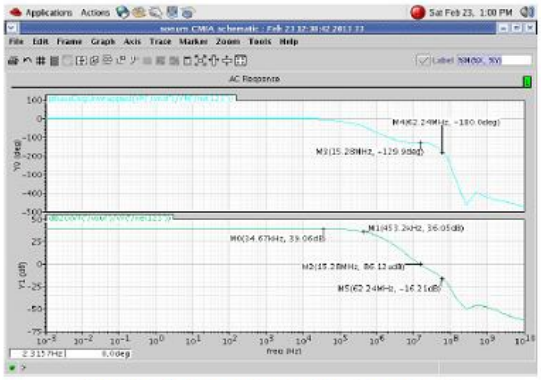

Figure 8. Frequency Response of Instrumentation Amplifier

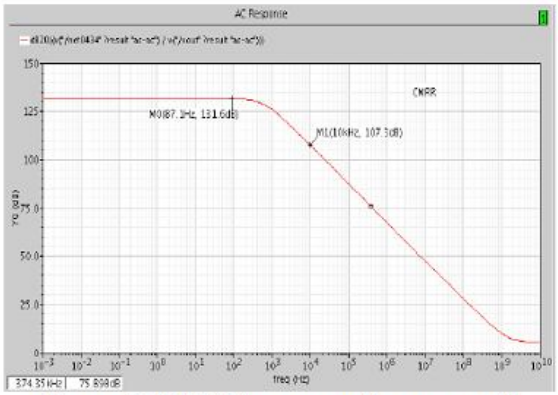

Figure 9. CMRR Frequency Response of Instrumentation Amplifier

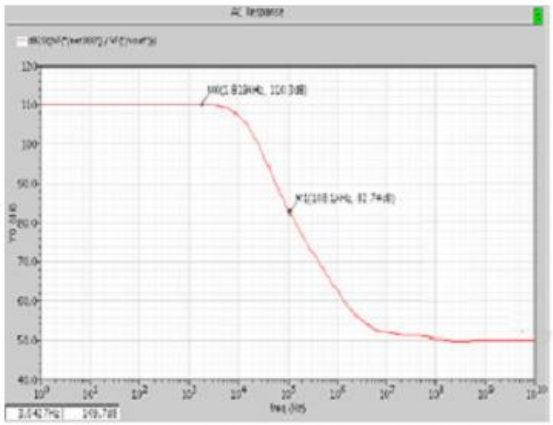

Figure 10. PSRR Frequency Response of Instrumentation Amplifier

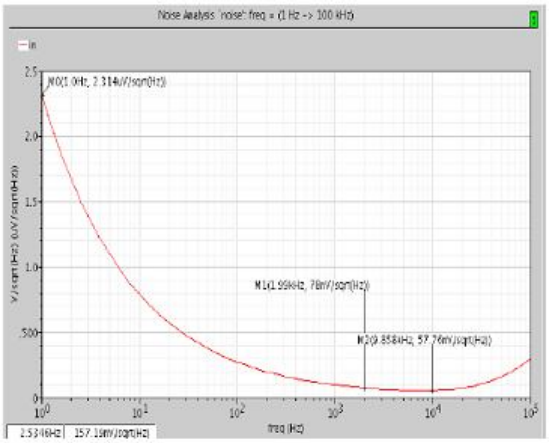

Figure 11. Equivalent input noise of Instrumentation Amplifier

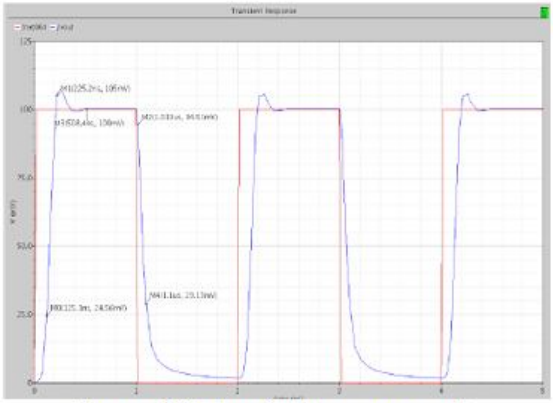

Figure 12. Transient response of Instrumentation Amplifier

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