

AN ECG INSTRUMENTATION AMPLIFIER WITH IMPROVED CMRR AND GAIN USING .18 μ M TECHNOLOGY

¹JYOTIDANGI, ²R.C. GURJAR

^{1,2}Electronics and Instrumentation Department SGSITS Indore

Abstract- This paper describes design of ECG instrumentation amplifier. Proposed instrumentation amplifier is a device created from operational amplifier. Its features are 141.61 dB CMRR, 54.83 dB gain and 223Hz bandwidth. Design and simulation of instrumentation amplifier is done using cadence environment with UMC 0.18 μ m CMOS technology at 1.8 V dual power supply.

Index Terms- ECG, Common mode rejection ratio, and Instrumentation amplifier.

I. INTRODUCTION

Recording the biomedical signal is one of the challenge in a biomedical detection system because the biomedical signal has very weak amplitude and low frequency e.g. in the range of 100 μ V to 5mV and \leq 1kHz [1]. Frequency and amplitude characteristics of biomedical signals [2] are shown in figure 1. Moreover common mode signal might be larger than of biomedical signal therefore high CMRR is required in any instrumentation amplifier IA to faithfully sense of the weak biomedical signals [3]. Usually an instrumentation amplifier with high CMRR and configurable differential gain characteristic used to extract the biomedical signals from human body. The IA is usually required to have a CMRR at least more than 100 dB and differential gain around 40 dB [4].

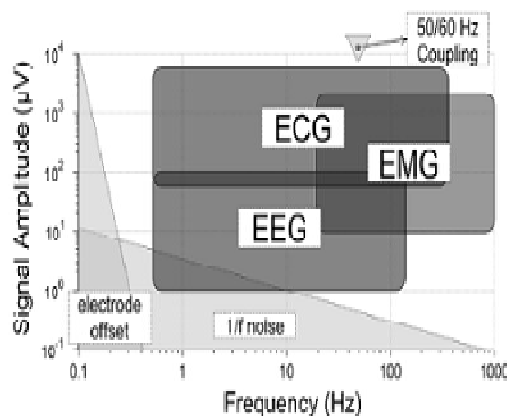


Figure 1. Frequency and amplitude characteristics of biomedical signals, and the nearby contaminating signals.

ECG signals are time varying signals, heart can be viewed as a time varying voltage source and voltage vary periodically based on cardiac cycle. Net voltage amplitude of ECG signal is the summation of the various cardiac cells potential [5] as shown in figure 2. For creating ECG signal on Cadence, Vpwl (piece wise linear file) source is used to create pwl file. Creating arbitrary waveform in cadence is tedious and

changes are difficult. Pwl files are text files with row of time/value pairs. ‘Time’ and ‘Value’ are separated by a space, each pair is on a separate line. Such files can easily be generated with Matlab/Octave, Excel (save as txt file) [6].

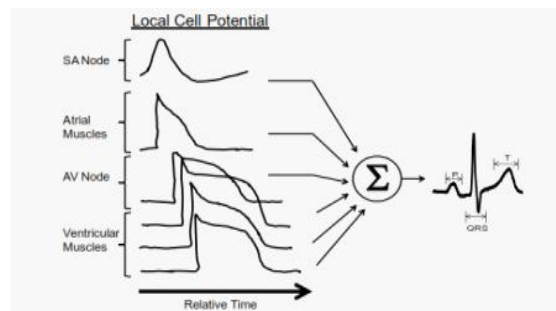


Figure 2. ECG signal

II. SYSTEM ARCHITECTURE

The overall system architecture of ECG measurement system is shown in figure 3. In ECG measurement system 12 electrodes (6 frontal and 6 transverse leads) are placed at multiple places on the body surface. These electrodes measures potential difference across a lead (i.e. a pair of electrode) and obtained raw ECG signals often low in amplitude and distorted by noise source, problem with having poor signal quality, hard to obtain physiological insights [5]. So for better response a high CMRR amplifier is used. Specification of amplifier are given in the table 1 .

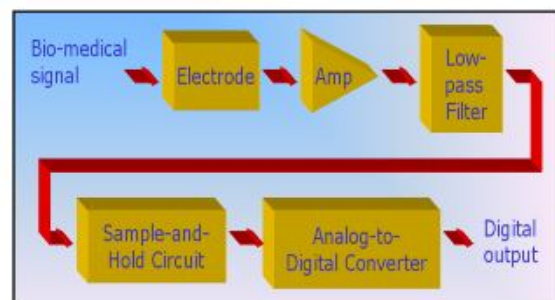


Figure 3. ECG measurement system

III. PROPOSED AMPLIFIER

TABLE 1: AMPLIFIER SPECIFICATION FOR ECG SIGNAL

PARAMETERS	SPECIFICATIONS
TECHNOLOGY	0.18μm
SUPPLY VOLTAGE	1.8V
GAIN	≥40 dB
CMRR	≥100dB
BANDWIDTH	150Hz

An instrumentation amplifier is an amplifier of electrical system to amplify small differential voltages. Due to the differential signals interferes are often generated in the form of common mode voltages. An amplifier with high common mode rejection ratio (CMRR) is suitable for biomedical application. Figure 4 illustrate the structure of proposed instrumentation amplifier. The IA consists of three op-amps and resistor network. the advantage of such an IA are: high input impedance , low input noise, and high CMRR with resistive feedback. First two op-amps are connected in the non-inverting follower stage, while third op-amp is the simple differential amplifier [1].

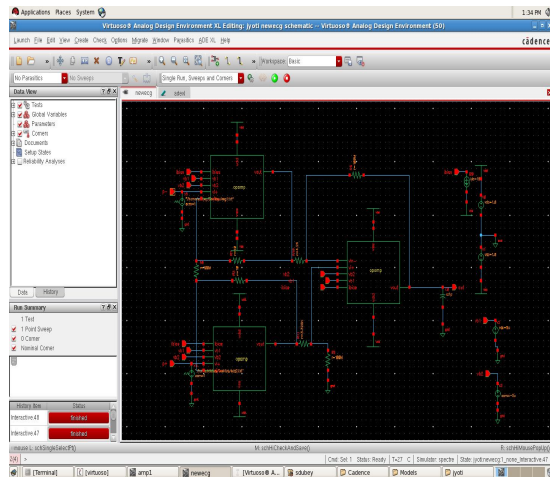


Figure 4. Schematic of proposed ECG amplifier

IV. PROPOSED OP-AMP

The two-stage CMOS operational amplifier includes four major circuitries—a bias circuit, an input differential amplifier, a second gain stage, and a compensation circuit. Figure 5 shows the block diagram of op-amp. The input differential amplifier block forms the input of the op amp and provides a good portion of the overall gain to improve noise and offset performance. The second gain circuit block is typically configured as a simple common-source stage so as to allow maximum output swings. The bias circuit is provided to establish the proper operating point for each transistor in its saturation region. The purpose of the compensation circuit is to maintain stability when negative feedback is applied to the op amp. Figure 5 shows the block diagram of the op amp circuit [7].

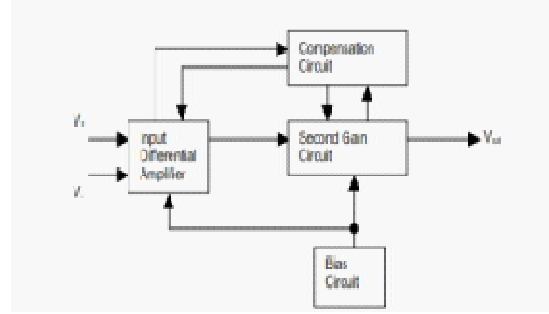


Figure 5. Block diagram of the op amp

The operational amplifier developed here is unbuffered (output resistance will be high), might be better name it, operational transconductance amplifier (OTA). Consider schematic of an unbuffered two stage CMOS op amp with p-channel input pair; usually have small amplitude and low frequency i.e. in the range of 100μV to 5mV and less than or equal to 1 kHz [8]. Figure 6 shows the schematic diagram of two stage op-amp.

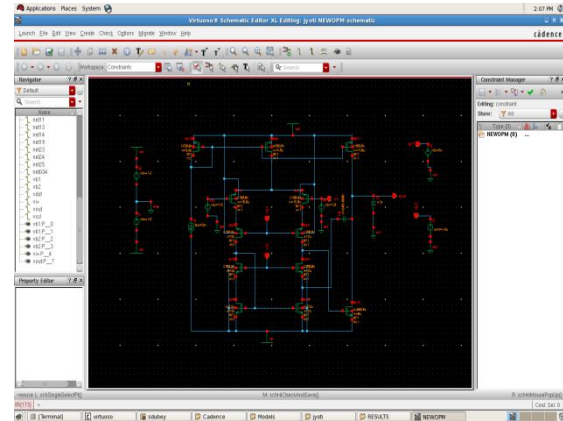


Figure 6. Schematic of two stage op-amp.

In op-amp load capacitor C_L of 1pF and compensation capacitor C_C of 208fF. In this analysis biasing voltages V_{b1} and V_{b2} are 5μV and -5μV respectively. And biasing current I_{bias} is 15nA. The table 2 shows the dimensions of each transistor in the circuit.

TABLE 2. W/L OF OP-AMP TRANSISTORS FOR ECG AMPLIFIER

DEVICES	W/L (μm)
M1,M2	15/0.18
M3,M4,M5,M6	2/0.18
M7,M8	2/3.5
M9	6.8/0.18
M10	2.8/0.18
M11	11/0.18
M12	8/0.36

V. SIMULATION RESULTS

A. TRANSIENT ANALYSIS

The simulated transient analysis of the V_{in} verses time and V_{out} verses time is shown in the figure. Applied

ECG input signal in range of 100μV to 5mV. In this analysis biasing voltages Vb1 and Vb2 are 5μV and -5μV respectively. And biasing current I_{bias} is 15nA. Transient response of proposed instrumentation amplifier has been analyzed by applying various input signals.

1) TRANSIENT RESPONSE FOR SQUARE WAVE

Square waves are applied as input of instrumentation amplifier and simulated input output response is shown below in figure 7.

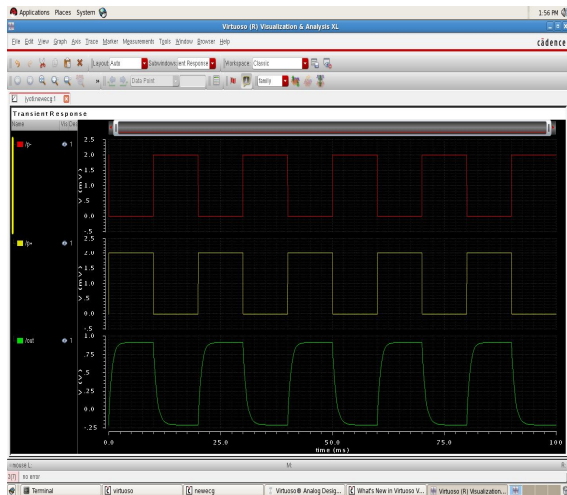


Figure 7. Transient analysis of instrumentation amplifier with square wave input

2) TRANSIENT RESPONSE FOR SINUSOIDAL WAVE

Sinusoidal waves are applied as input of instrumentation amplifier and simulated input output response is shown below in figure 8.

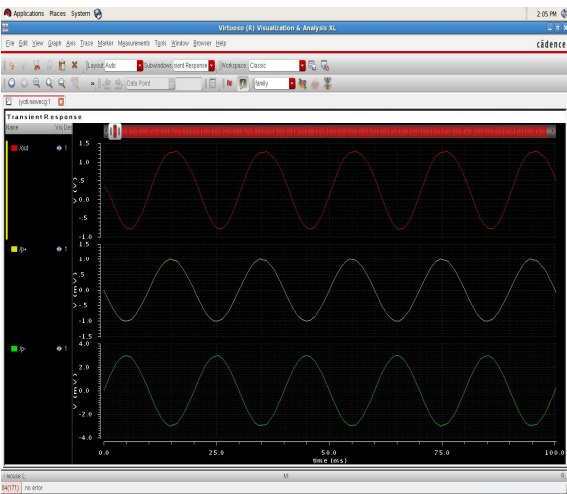


Figure 8. Transient analysis of instrumentation amplifier with sinusoidal wave input

3) TRANSIENT RESPONSE WITH ECG INPUT

ECG signals are applied as input and simulated input output response is given below in figure 9.

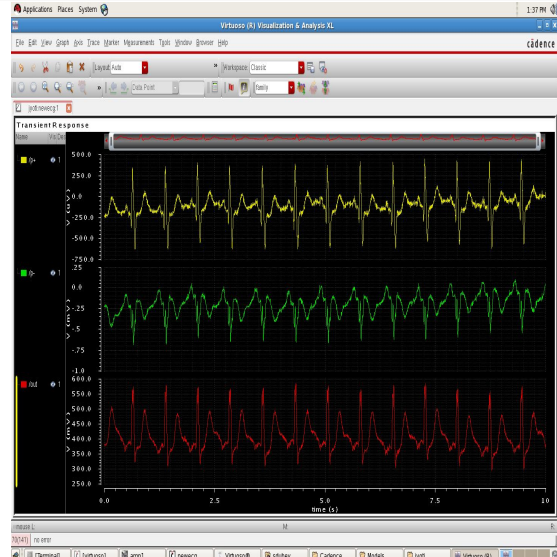


Figure 9. Transient analysis of instrumentation amplifier with ECG input

B. AC ANALYSIS OF PROPOSED INSTRUMENTATION AMPLIFIER

AC analysis has been done for proposed instrumentation amplifier circuit. In this case, biasing voltages and current are remaining same. And other important parameters such as gain, phase response, CMRR are measured. Figure 10 shows the gain and phase response of instrumentation amplifier.

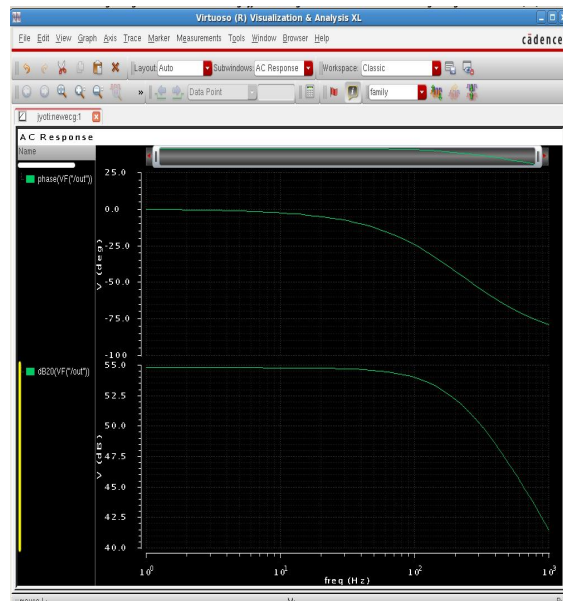


Figure 10. Gain and phase plot of instrumentation amplifier

CMRR of amplifier is the ratio of differential mode gain and common mode gain. CMRR of an amplifier will be very high and ideally infinite. Thus common mode gain of amplifier will be very low. Figure 11 shows common mode gain of instrumentation amplifier. Differential gain (A_d) of instrumentation amplifier is 54.83dB and common mode gain (A_c) is -86.78dB, so the CMRR is 141.61dB. $CMRR (dB) = 20\log (A_d/A_c)$.

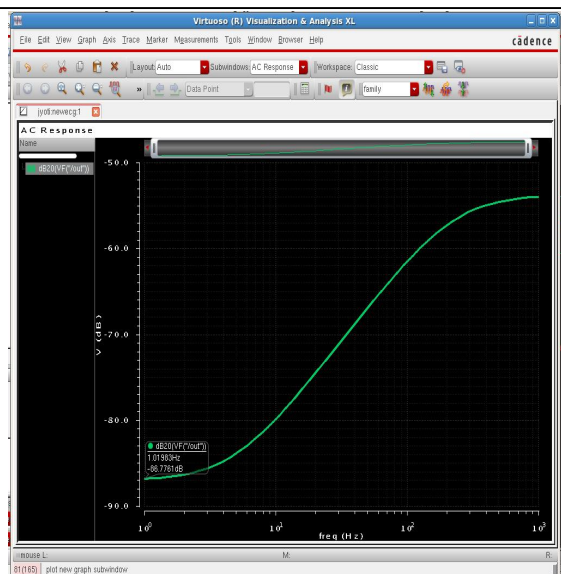


Figure 11. Common mode gain of instrumentation amplifier

TABLE 3: RESULTS AND COMPARISON

PARAMETERS	SPECIFICATION	SIMULATION RESULTS
Biasing current	-	15nA
Gain	≥ 40 dB	54.83dB
CMRR	≥ 100 dB	141.61dB
Bandwidth	150Hz	223Hz

CONCLUSION

The circuit simulated in cadence with UMC 0.18 μ m CMOS technology. Results are shown in table 3. The instrumentation amplifier operates with the 1.8V double power supply. Simulation results with 54.83dB of gain, 141.61dB of CMRR and 223Hz bandwidth are obtained. Proposed IA can be used as amplifier in an ECG acquisition system.

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REFERENCES

- [1] Hwang-Cherng Chow and Jia-Yu Wang "high CMRR instrumentation amplifier for biomedical application" IEEE 2007.
- [2] Ahmed N. Mohamed, Hesham N. Ahmed, Mohamed Elkhatab "A low Power Low Noise Capacitively Couple Choppe Instrumentation Amplifier in 130 nm CMOS for Portable Biopotential Acquisiton Systems " IEEE 2013.
- [3] Chia-Hao Hsu and Chi-Chun Huang "A High Performance Current-Balancing instrumentation Amplifier for ECG Monitoring" IEEE 2009.
- [4] Jin Tao Li, Sio Hang Pun, Peng Un Mak and Mang I Vai "Analysis of Op-Amp Power-Supply Current Sensing Current-Mode Instrumentation Amplifier for Biosignal Acquisition System " IEEE 2008.
- [5] Dr. Alfred Yu "IEEE-RWEP_Electrocardiogram Am_Bkgrd-Lect ".
- [6] Brandon Romberg "cadence tool" WestVirginia University.
- [7] Shunping Wang, Yiping (Neil) Tsai "CMOS operational amplifier" The George Washington University 2007.
- [8] Ehsan Kargaran, Hojat Khosrowjerdi, Karim Ghaffarzadegan "A 1.5 V High Swing Ultra-Low-Power Two Stage CMOS OP-AMP in 0.18 μ m technology" 2010 IEEE.
- [9] Dr. Ahmad Khateb, "Step BY STEP CADANCE MANUAL AND EXAMPLES Schematic".
- [10] <http://physionet.org/cgi-bin/atm/ATM>.

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