POWER ANALYSIS OF CMOS AND ADIABATIC LOGIC DESIGN

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Abstract- The main objecive of this paper is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Then, to limit the power dissipation, alternative solutions at each level of abstraction are proposed. The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this paper, a new CMOS logic family called ADIABATIC LOGIC, based on the adiabatic switching principle is presented. The Logic cells like 2N2P, 2N2N2P, PFAL has been designed and presented here. Power consumption is widely reduced upto50%. The simulation tool used to design Adiabatic cell is TANNER EDA V13.0 Technology.

Keywords- Adiabatic, Cmos, low power Very Large Scale Integration,2N2N-2P, PFAL.

I. INTRODUCTION

Demands for low power circuits have motivated VLSI designers to explore new approaches to the design of VLSI circuits. Adiabatic logic means energy recovery logic.

Adiabatic circuits achieves low energy dissipation by restricting current flow across devices with lower voltage drop and by recycling the energy stored on their capacitors.

Adiabatic logic also generates low switching noise. In mixed signal analog and digital IC design switching noise is an important problem. In adiabatic circuits switching occurs with minimum voltage drop across devices and node's voltages changes slowly.

Youmis and Knight have proposed adiabatic logic families with less power dissipation but each gate requires 16 times the number of devices compared to conventional logic.

In this paper we have used 2N2N-2P and PFAL adiabatic logic family

II. DESIGN:

A)CONVENTIONALDESIGN:

a)CMOS INVERTER:

The first basic cell which the VLSI designers implements and analyze is the basic CMOS Inverter. Here also this thesis work starts with the designing of the basic CMOS Inverter of minimum transistor size.

The basic structure of a CMOS Inverter is shown in Figure 1 & the transient simulation results are as shown Figure 2.

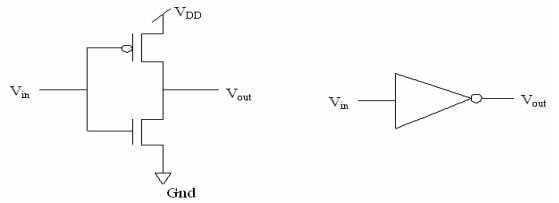

Figure 1. The Basic Structure of CMOS Inverter.

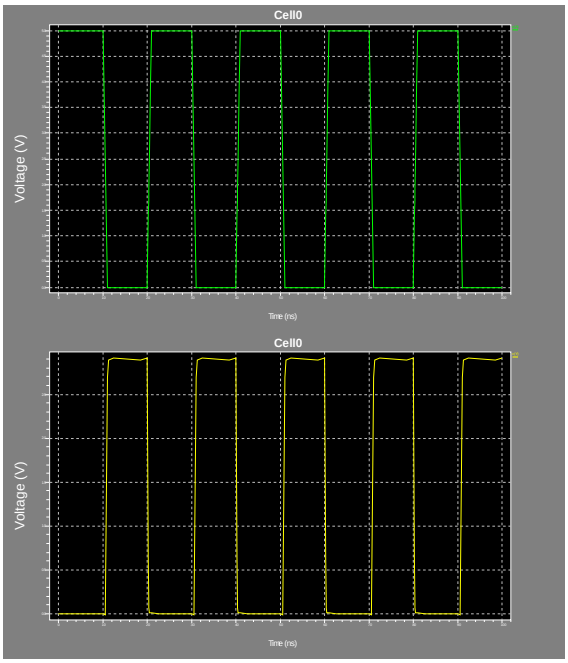

Figure 2. Voltage waveform of Cmos Inverter

b) CMOS NAND GATE:

The next basic cell to consider is the CMOS-based Two-Input NAND Gate, designed and simulated in the standard Tanner tool CMOS Technology. The minimum sized NMOS and PMOS transistors have been used for the transient simulations. The basic structure and transient simulation results are as shown in the below Figure 3&4.

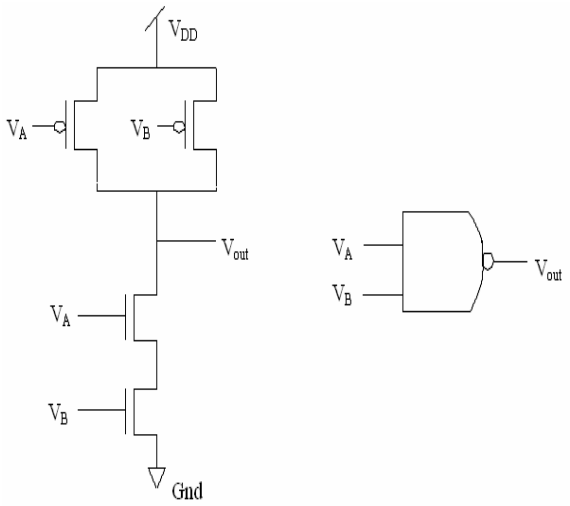

Figure 3. The Basic Structure of a Two-Input CMOS NAND Gate.

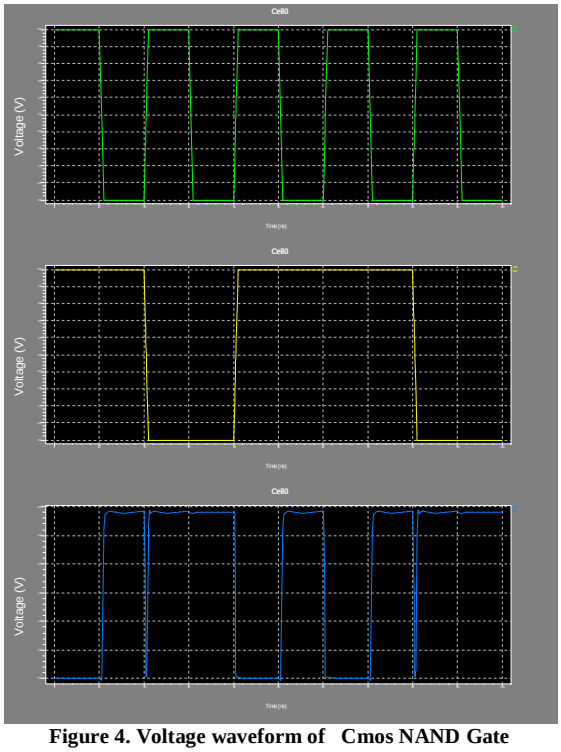

Figure 4. Voltage waveform of Cmos NAND Gate

B)PROPOSED ADIABATIC LOGIC DESIGNS
a). 2N2N-2P INVERTER

The 2N2N-2P adiabatic block has a 2N2P latch which consists of two NMOS and two PMOS transistors, along with complementary functional blocks, in parallel with the two NMOS devices of the 2N2P latch. The presence of these NMOS transistors avoids the occurrence of floating nodes with remnant charge, which will pay way for charge sharing and leakage. This ultimately results in loss of high frequency performance of the circuit. The four main phases of operation of the 2N2N-2P logic gates are 1)input, 2) hold, 3) recovery and 4) reset. A typical 2N2N-2P inverter is shown in Fig. 5, to briefly explain the operation of the circuit.

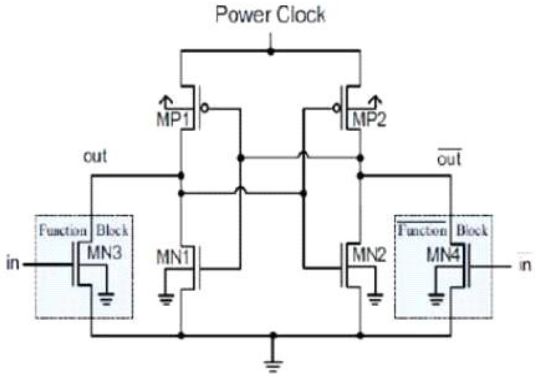

Figure 5. Inverter using 2N2N-2P logic

A four- phase power-clock is employed to power the circuit.It is called as power-clock to identify the fact that these power-clocks power the circuit and act as the timing clocks for the pipelined adiabatic circuit. By pipelining, we mean the operating nature of the adiabatic circuits, wherein the output of the current stage when held, is used for evaluation by the next stage in the circuit, and signal goes on across the stages by the presence of power-clock signals, each lagging behind the previous by 90o which is shown in figure 5.To explain the buffer operation, consider an input is applied, when the power-clock is low. Note that the complementary input from the previous stage is applied. This makes MN3 to conduct pulling the node out to zero. At this time, MN4 does not conduct. During the evaluation phase the power-clock (PC) rises and when the PC voltage reaches above the threshold voltage of PMOS device MP2 starts conducting.Node outbar gets charged as MP2 conducts and it follows the power-clock. During the hold phase, the outputs are maintained the same. In this phase of operation, the next stage of adiabatic circuit, operates in its evaluate phase. During the recovery phase, power-clock starts falling. Then, since the node outbar is at a higher potential than the power-clock voltage,the charge from outbar goes back to the power-clock and hence energy is recovered.

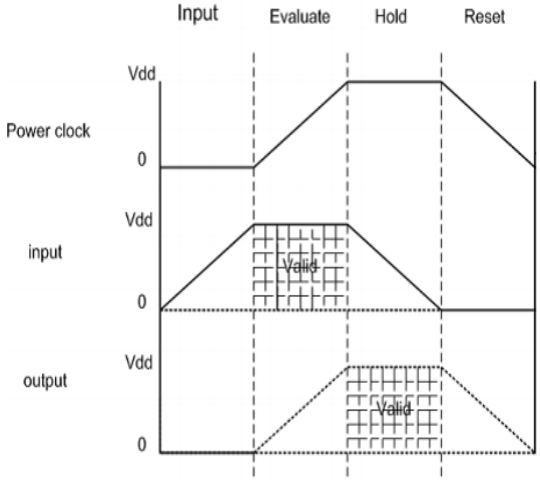

Figure 6. Timing Diagram for 2N2N-2P logic

The transient simulation results are as shown in the Figure 7

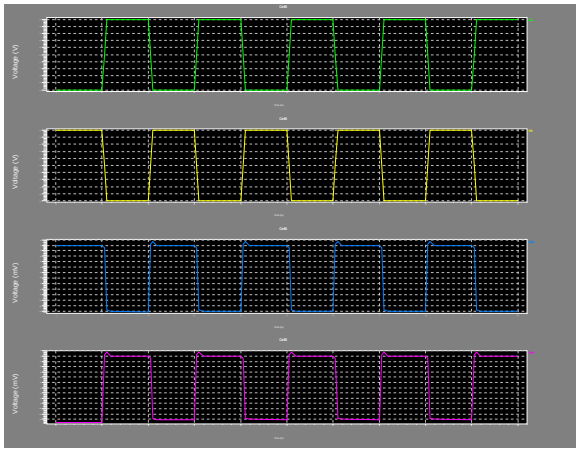

Figure 7.Voltage waveform of 2N2N-2P Inverter.

b) Adiabatic Two Input 2N2N-2P NAND GATE

The adiabatic 2N2N-2P two-input NAND/ AND gate can be implemented as shown below in the Figure 7 using standard Tanner Tool technology and simulated waveforms is shown in Figure 8, respectively.

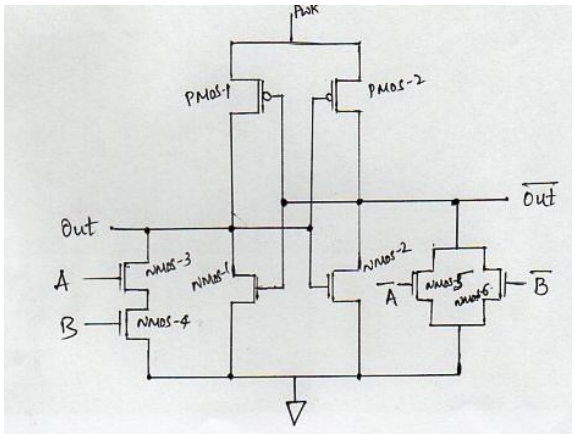

Figure 8.Basic Structure of Two input 2N2N-2P NAND Logic

The transient simulation waveform results are shown in the figure

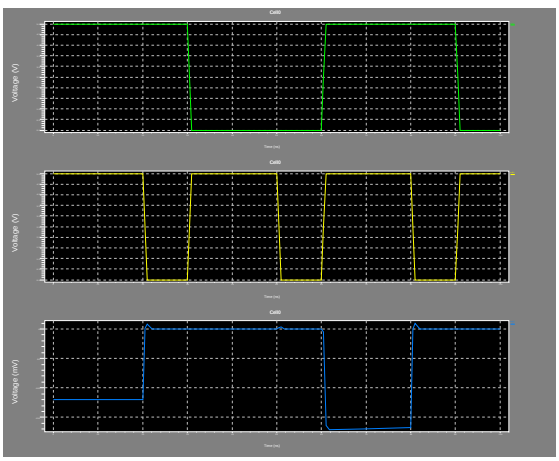

Figure 9.Voltage waveform of 2N2N-2P NAND Logic

C) PFAL

The acronym PFAL stands for the Positive Feedback Adiabatic Logic. It is a dual rail adiabatic circuit capable of realizing partial energy recovery. The basic circuit of Fig. 9 represents a buffer implemented using PFAL logic.

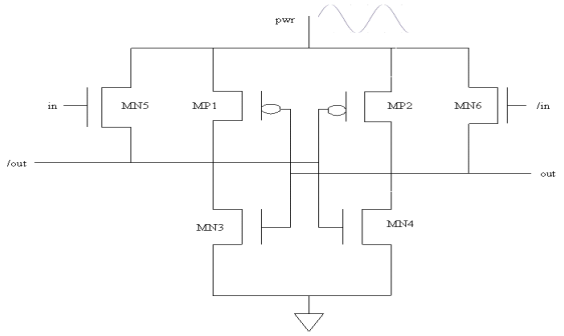

Figure 9. The basic structure of PFAL Inverter

Analogous to the 2N2N-2P logic, this logic also uses the four-phase power-clock, consisting of 4 phases, namely, (1) the rising phase of power-clock called evaluate, (2) the constant phase called hold, when the output is held for the next stage to evaluate this signal, (3) the falling phase of power-clock called reset or recovery, where the process of charge reclamation or charge retrieval takes place. This is followed by the Wait phase, which synchronizes the flow of data across the adiabatic pipeline.

The heart of the PFAL circuits is the adiabatic amplifier latch made by two PMOS and NMOS transistors. The main difference between the PFAL and the 2N2N-2P logics is that the complementary functional blocks in PFAL are implemented as a pull up network, in parallel with the two PMOS devices. This has its characteristic advantages and disadvantages, when compared to the 2N2N-2P logic. This is explained in the following paragraph.

During the evaluate phase of the power-clock, assume that the input out is already high and /out low. When the powerclock voltage level rises above the threshold voltage Vtn of the NMOS transistor, the transistor MN5 conducts and connects the rising node voltage /out to PC. This node /out with rising voltage turns on the device MN2 and pulls the node out to ground. This in turn is applied to the gate of the PMOS device MP1. This in effect realizes a parallel combination of the PMOS and NMOS devices, namely, MN5 and MP1. This results in reduced ON resistance through the transmission gate structure. This reduction of resistance is the main advantage of the PFAL. During the hold phase of the power-clock, the out and /out logic levels are used as the input for the succeeding gate of the adiabatic pipeline. During the recovery phase, the power-clock voltage reduces. Then, due to the potential difference existing between the power rail and out node, the charge gets transferred back to the PC. However, since the input

NMOS device at this time is OFF, energy recovery is made possible only through the PMOS device. This in effect poses increased resistance. When the PC voltage is lower than the Vth of the PMOS device, the charge recovery stops. This results in the floating node problem, due to the remnant charge. This remaining charge is retained in the output node and is dissipated in the next stage, when the states of the adiabatic stage change. Hence, this logic falls under quasi adiabatic family, that is complete recovery of energy is not possible due to the losses mentioned above. The floating output node problem also results in poorer high frequency performance The Transient simulation results of PFAL inverter is as shown in below figure 10

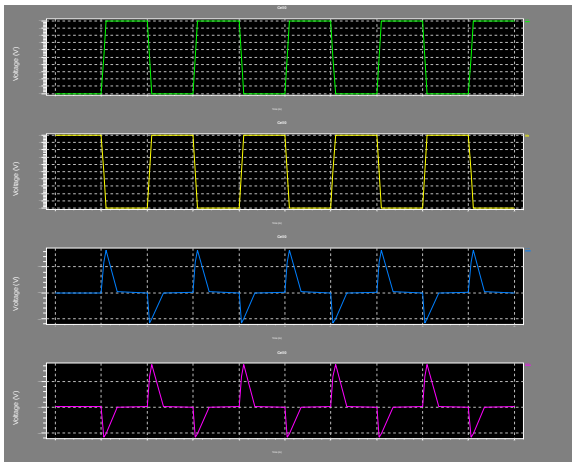

Figure 10. Voltage waveform of PFAL Inverter

d) Adiabatic Two Input PFAL NAND GATE

The partially adiabatic PFAL two-input NAND gate can be implemented as shown below in the Figure 11 using standard Tanner Tool technology and simulated waveforms is shown in Figure 12, respectively.

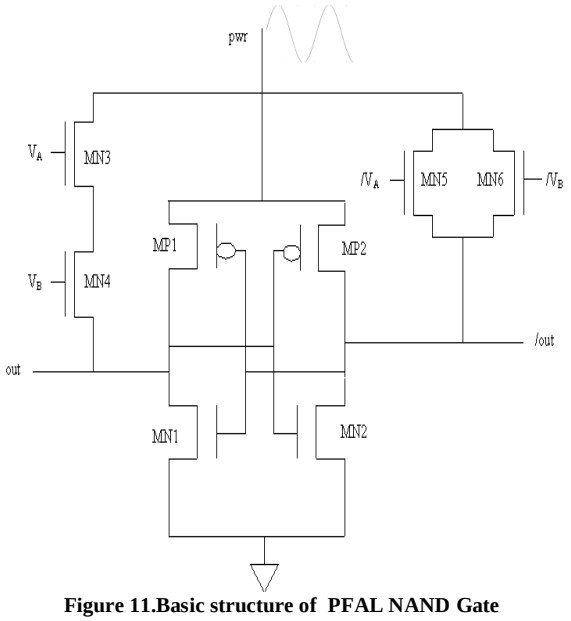

Figure 11.Basic structure of PFAL NAND Gate

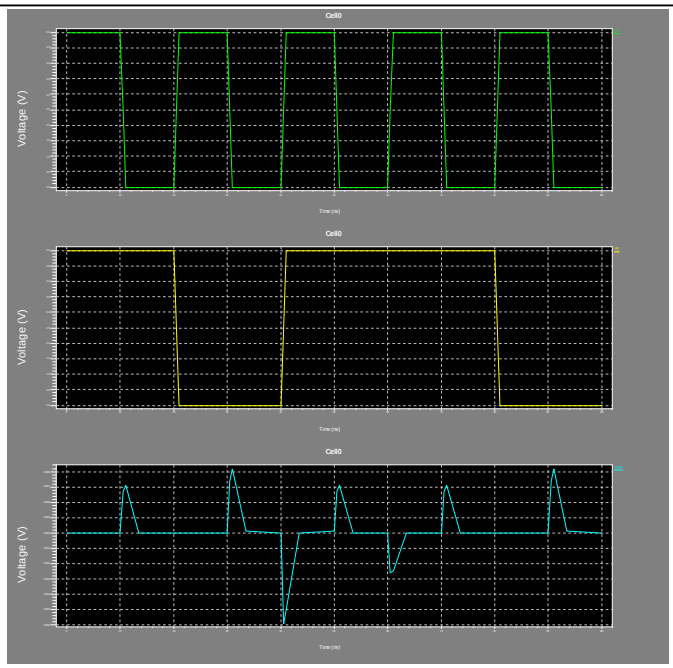

Figure 12. Voltage waveform of PFAL NAND Gate

III. RESULTS AND DISCUSSIONS

This section deals with the comparison of the full complementary CMOS logic style with the ultra low-power adiabatic logic style.

Table I&II depict the power comparison made for the proposed inverter and nand gates constructed using 2N2N-2P and PFAL adiabatic structures. The analysis is made for various voltages across a range of 2.9V to 3.3V, to validate the design.

TABLE I
POWER COMPARISON AT DIFFERENT VOLTAGES

Inverter Type	Power consumption in micro watts				
	2.9v	3v	3.1v	3.2v	3.3v
CMOS INVERTER	16.7	20.6	25.3	32.1	32.5
2N2N-2P INVERTER	0.505	0.607	0.718	0.841	0.974
PFAL INVERTER	0.497	0.596	0.628	0.707	0.971

TABLE II
POWER COMPARISON AT DIFFERENT VOLTAGES

	Power consumption in micro watts				
	2.9v	3v	3.1v	3.2v	3.3v

CMOS NAND Gate	25.05	28.89	31	31.38	38.14
2N2N-2P NAND Gate	0.665	0.772	0.889	1.018	1.15
PFAL NAND Gate	0.459	0.555	0.639	0.785	0.922

In Table III shows the transistor count in various adiabatic architecture for inverter and NAND gate in comparison with CMOS inverter and NAND gate. It is found that our proposed Adiabatic logic families uses more transistor count than compared to CMOS .In spite of using more transistor count than CMOS there is significant reduction in power consumption as compared to CMOS implementation .

TABLE III
TRANSISTOR COUNT COMPARISON OF VARIOUS INVERTERS

	NUMBER OF TRANSISTORS		
	CMOS	2N2N-2P	PFAL
INVERTER	2	6	6
NAND GATE	4	8	8

CONCLUSION:

In this paper we analyzed the power consumption of various circuit shown in above Table and comparison of performance of different adiabatic logic circuits with traditional CMOS circuits. The analysis shows that designs based on adiabatic principle gives superior performance when compared to traditional approaches in terms of power even though their transistor count is high in some circuits so for low power and ultra low power requirements adiabatic logic is an effective alternative for traditional CMOS logic circuit design.

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